SYSTEM AND METHOD FOR DERIVING SYMBOL TIMING

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority to and the benefit of co-pending U.S. provisional

5   patent application entitled, "Equalizer Derived Symbol Timing," filed on October 27,

1999 and accorded serial number 60/161,799 (Docket No. 61606-8220; 1999-12), which

is entirely incorporated herein by reference.

TECHNICAL FIELD OF THE INVENTION

10   The present invention generally relates to modem communications, and more

particularly to a system and method for deriving symbol timing in modems.

BACKGROUND OF THE INVENTION

In recent years there has been an exponential expansion in the Internet and in the

15   number of people who want to connect to the Internet. Businesses have found the

Internet a cheap and efficient way of communicating information to their customers, to

their suppliers, and even among their own workforce. Employees exposed to the Internet

at work have gone in search of tools to connect the personal computers they have at home

to the Internet so that they can have access to the vast resources they have become

20   accustomed to at work.

The modem has filled this need for the past twenty years, but in the past ten years

it has seen unprecedented advances in technology. With the advent of the World Wide

Web associated with the Internet, engineers have consistently needed to push larger and

larger amounts of data through a pipeline that has not really grown. In the past few years,

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with demand growing for "real-time" networks, designers have started to develop alternatives to the traditional modem after deciding that traditional modems most likely had a top speed around 56Kbps. These include digital subscriber line (DSL) modems, integrated services digital network (ISDN), and cable modems.

5   DSL modems in particular have received a lot of attention recently. DSL modems operate at higher data rates through a combination of higher frequency transmission and by using mapping techniques to map a series of bits onto a single symbol. These techniques typically require that both the transmitter and receiver are in sync with each other. When the systems are not in sync, either or both of the receivers are looking at an

10   incorrect portion of the signal. In such a situation, the systems are likely to see an incorrect phase angle or an incorrect magnitude, and the data ends up being misinterpreted.

In the past, synchronization has been done either through the use of a preamble, the use of an off frequency pilot tone or analysis of band edge signals. Using the

15   preamble method, a known set of data is transmitted at the beginning of each transmission, and the receiver looks for this set of data and determines the characteristics of the transmission. The pilot tone method on the other hand, transmits a constant pattern of data (pilot tone) offset from the carrier frequency, thus allowing the receiver to derive the timing information from the pilot tone even in the absence of modulated data. The

20   band edge method filters the signal at each edge of the modulated bandwidth then performs non-linear operations to measure the bandwidth or symbol rate. Each of these systems has certain disadvantages.

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SUMMARY OF THE INVENTION

The present invention involves an improvement to a receiver of a modem in a half-duplex multi-point or point-to-point system or full duplex system that enables elimination of both the pilot tone and the preamble by deriving the symbol timing directly from the equalized or demodulated symbols. By employing the present invention, modems are able to derive the incoming symbol timing from the received symbols. By deriving the symbol timing dynamically, the modem will conserve power over the pilot tone and make special start up preamble signals unnecessary, thereby reducing the time required to communicate data.

When the symbol timing derivation system is used in a multiple virtual lines (MVL) system, as an example, the invention uses a forward equalizer to clean up the signal, then the frequency is locked and the phase corrector rotates the constellation to the correct orientation for the slicer. The discrete data symbol produced by the slicer, which may include advanced data recovery techniques, is then rotated back into its original orientation and subtracted from the pre-sliced signal and sent back to the forward equalizer to update the equalizer coefficients.

However, the invention can also be applied to, as another example, discrete multi-tone (DMT) systems, by using the received symbols to derive symbol timing. Here the symbol timing derivation system is very similar, but does not include a decision feedback equalizer or a centroid error calculation, and replaces the non-linear decoder with a discrete Fourier transform (DFT) and a switch to handle the numerous carriers present in DMT.

The receiver includes a voltage controlled crystal oscillator (VCXO) which controls receiver timing and could allow the remote modems to transmit to the control

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modem using a time base that is in sync with the received symbol timing. This reduces the need for timing correction or tracking in the equalizers at either end of the line.

The present invention can also be conceptualized as providing a method for communication in a modem. This method can be broadly summarized by the steps of: decoding a received signal segment into a discrete data symbol, calculating a timing phase error and an average timing phase error based upon the received signal segment and discrete data symbol, creating a control signal based upon the average timing phase error, and generating symbol timing for a receiver based upon the control signal.

Other systems, methods, features, and advantages of the present invention will be or become apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional systems, methods, features, and advantages be included within this description, be within the scope of the present invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

This invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being place on clearly illustrating the principles of the present invention. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

FIG. 1A is a block diagram of a first embodiment of the symbol timing derivation system of the present invention, which is situated in a DSL modem of a point to point system.

FIG. 1B is a schematic diagram of the first embodiment of FIG. 1A.

FIG. 2A is a block diagram of the second embodiment of the symbol timing derivation system of the present invention, which is situated in a multi-point system.

FIG. 2B is a schematic diagram of the second embodiment of FIG. 2A.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1A shows a schematic view illustrating a point-to-point communications system 11 in which modems 13, 15, employing the concepts and features of a symbol timing derivation system, are used. Remote computer 14 and its DSL modem 13 is

10 connected to a central office (CO) 16 via communications channel 12. Located at a central office 16, is DSL modem 15. The channel 12 can be a wire or wireless link, but is typically, although not necessarily, the copper wire pair that extends between a telephone company central office and a remote residential business, or any other location served by local telephone service. Remote computer 14 can be located at a residence, business, or

15 any other location served by conventional copper wire pair where DSL modems 13, 15 may currently be used. By using modem 15 and modem 13 employing the concepts and features of the symbol timing derivation system 17, it is possible to derive symbol timing without the use of a symbol preamble or pilot tone. This feature allows both modems 13, 15 to maintain synchronization with each other, and advantageously conserve energy

20 while maximizing data rate.

Now referring to FIG. 1B, shown is a schematic view illustrating the symbol timing derivation system 17 belonging to DSL modem 13 and/or DSL modem 15 of FIG. 1A including the concepts of the present invention. The transmitter 18 of modem 15 first

transmits a signal across the channel 12, which is modeled here by the addition of a phase

rotation 22, φ, and additive noise 23, n, from the line, to the receiver 19 of a remote

modem 13. This embodiment of the symbol timing derivation system 17 begins with the

forward equalizer 24. The forward equalizer 24 takes the incoming signal and uses its

5   coefficients to clean up the signal by removing intersymbol interference and reducing

signal noise.

Once the forward equalizer 24 has adjusted the signal, the symbol timing

derivation system 17 allows for a non-linear decoder 25, the use of which is described in

US Patent number 5,265,127 to Betts, *et al.* which is hereby incorporated by reference.

10   The non-linear decoder 25, however, is not included in the preferred embodiment. When

operating in a discrete multi-tone (DMT) system, which is well known in the art, this

non-linear decoder block 25 would be replaced by a Discrete Fourier Transform (DFT)

producing numerous outputs in the frequency domain. These numerous outputs

correspond to the different multi-tone carrier frequencies of the received signal. A switch

15   controls which carrier is fed into the symbol timing derivation system 17 at any instant in

time.

In the next step, the results of the decision feedback equalizer 33 are subtracted 26

from the incoming signal. This step allows the receiver to subtract 26 from the signal any

past signals that may have seen time dispersion as a result of the channel. The resulting

20   signal, eq_xeye 27, is then fed to three different components.

The first component to be discussed will be the slicer 29. The signal, eq_xeye 27,

is first phase rotated by $-\varphi'$ 28. This phase rotation 28 puts the constellation in the

correct (squared up) orientation for the slicer 29, so that the slicer 29 does not

misinterpret the signal as being in an incorrect decision region due to phase error. The slicer 29 then decides where the constellation point lies. Additionally, any advanced data recovery techniques, such as well known trellis coding, may be applied in the slicer 29. The slicer 29 then produces a reference signal 30 in the form of a discrete data symbol,

5   which locates the constellation point at the center of a decision region. It should be appreciated that the above description of a slicer 29 should not limit the symbol timing derivation system 17 to operate only on quadrature amplitude modulated systems. The slicer 29 should be interpreted as a decision function in any modulation technique to decide where a signal should be interpreted to be located, including any amplitude shift

10   keying, phase shift keying, or frequency shift keying techniques, or any combination thereof. The reference signal 30 is then phase rotated 31 back to its original orientation. The resultant signal 32 then updates the decision feedback equalizer (DFE) 33 and the phase corrector 36, although when operating in DMT, the symbol timing derivation system 17 could operate without a DFE 33. Even in DMT though, the symbol timing

15   derivation system 17 can benefit from the inclusion of a noise whitening DFE 33 to further refine the signal.

The inputs to the DFE 33 include the sliced signal (X'_r, Y'_r) 32, minus the unsliced signal 27, which indicates the error present in the DFE compensated signal, and the sliced signal 32 minus the result of the forward equalizer 24 delayed by one cycle,

20   which shows both channel dispersion and signal noise. The result of the sliced signal 32 minus the unsliced signal 27 also results in the update error 34, which is sent to the forward equalizer 24 to update its coefficients. With respect to the second input to the DFE 33, one skilled in the art will recognize that this subtraction 35 can also occur after

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the delay, with the caveat that the corresponding signal 32 needs to be properly synchronized. The DFE 33 in this embodiment is a noise whitening DFE 33, and decides what part of the signal is due to noise 23 from the channel 12 and subtracts 26 the noise 23 from the output of the forward equalizer 24.

5   The use of a phase corrector 36 is known in the art. An example of a phase corrector can be seen in U.S. Patent number 4,532,640 to Betts *et al.*, which is hereby incorporated by reference. The inputs to the phase corrector 36 consist of eq_xeye 27 and (X'_r, Y'_r) 32. The phase corrector 36 multiplies the signals 27, 32 together and multiplies the result by 2^{-4}, a scalar. The phase corrector 36 then combines the product to

10   the previous result (*e.g.*, integrates), sending the result 37, φ', to phase rotator 31 also to an inverter 38, which inverts the result 37 and sends it to phase rotator 28.

Finally, the eq_xeye signal 27 is used to derive the timing phase error. The equation for deriving the timing phase error is as follows:

$$t_e = y_e \cdot x_r - x_e \cdot y_r$$

15   where the result is the product of the constellation vector 27 and the reference vector 30. This result shows how much the eq_xeye 27 signal has rotated in relation to the ideal reference vector 30. As is known in the art, the circuit may use the phase rotated vector (X'_r, Y'_r) 32, to derive the timing phase error, the difference is that the phase corrector in such a circuit will be a 360 degree phase corrector. In contrast, the present embodiment

20   utilizes a phase corrector 36 that can correct up to one radian of error. Back to the present embodiment the timing error resulting from multiplier 39 is then multiplied by a scalar 40, 2^4 in this embodiment, and is input to a leaky integrator 41 which calculates the

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average timing phase error. The other input to the leaky integrator 41 is communicated from the centroid error 48 which is combined via adder 42 to the scaled timing phase error and integrated 41. It should be added that in DMT, there should be no centroid error calculation unless the DMT equalizer adaptively updates its coefficients.

5   Calculation of the centroid error 48 begins with the calculation of the centroid 44 itself. The centroid 44 is calculated according to the following equation:

$$Centroid = \frac{\sum i \cdot |C_i|}{N}$$

Where i is the equalizer coefficient index, C_i is the coefficient, and N is the total number of coefficients. The error is then calculated by sending the result of the centroid block 44

10   to a subtractor block 45, which subtracts the ideal signal 46 from the centroid. The centroid 44 may be the true centroid or the location of the largest magnitude equalizer coefficient. For a 36-coefficient equalizer, the ideal centroid 46 has been set at 19, which biases the equalizer to the high side of halfway. The subtraction result is then sent to a multiplication block 47, where it is multiplied by a scalar, β_C. In ideal conditions, the

15   centroid error 48 will be zero. However, when the centroid error 48 becomes non-zero, the centroid error 48 biases the leaky integrator, and thus the VCXO 57, to compensate for the movement of the equalizer coefficients so that the coefficients will move back to the center, or ideal position. Without the centroid calculation 44, the equalizer coefficients can make a random walk to either extreme, at which point the equalizer 24

20   can no longer correct for additional error in the signal.

The summation 42 result is then input to a subtractor 43 along with a scaled 50 version of the previous result delayed one cycle by the delay block 49. The result of the leaky integration 41 is as follows:

$$\varphi e_n = \left(1 - 2^{-4}\right)\varphi e_{n-1} + e_c + 2^{+4}t_e$$

5 where φe_n is the timing phase error, φe_{n-1} is the previous timing phase error, e_c is the centroid error 48, and t_e is the timing error computed above.

The final portion of the symbol timing derivation system to be discussed is the voltage controlled crystal oscillator (VCXO) 57 control circuit 51. This circuit 51 is comprised of a second order phase locked loop (PLL) 51 which develops the control
10 voltage for the VCXO 57. The output of the leaky integrator 41 described above is split and fed into two different multipliers 52, 53. The first multiplier 52 multiplies the signal by the scalar 2^{-2}, while the second multiplier 53 multiplies the signal by 2^{-16}. The output of this second multiplier 53 is then fed to an ideal integrator, which is made up of a summation block 54 and a delay element 55. The output of the ideal integrator 54 is taken
15 at the output of the delay element 55 and fed to a summation block 56, where it is added to the result of the first multiplier 52 to control the VCXO 57. The resulting equations are as follows:

$$VCXO = 2^{-2}\varphi e_n + \Delta f$$
and

$$\Delta f = \Delta f + 2^{-16}\varphi e$$

20 where φe is the timing phase error, and Δf is the second order frequency offset.

In an alternative embodiment shown in FIG. 2A, the symbol timing derivation system 66 is used in a multi-point system 60. FIG. 2A shows a central office DSL modem 61 with a transmitter 65 and a receiver 64, which contains the symbol timing derivation system 66, connected to many remote DSL modems 63, also equipped with a

5   transmitter 65 and receiver 64, and containing the symbol timing derivation system 66. The symbol timing derivation systems 66 of these DSL modems 61, 63 are shown in FIG. 2B. The novelty here is the dual eye closure 71, 72. The eye closure functions 71, 72 sense when no signal is present and opens the flywheel switch 73. Prior to the present embodiment 66, DSL modems only included one eye closure 71. What prior

10   embodiments did not consider, however, is that even when no signal is present, the DFE 33 might create a signal, thus eye close 71 might not realize that no signal is present. Therefore, a second eye close 72 was added to detect when no signal was present coming out of the forward equalizer 24. Eye close 71 is still used, though, because it takes advantage of both the DFE 33 for noise reduction, and the phase corrector 36, to rotate

15   the signal back to the correct orientation. The eye closures 71, 72 may be used in point-to-point systems 11 running in full duplex, to correct for carrier dropout, but is normally used when running half duplex in either point-to-point 11 or multi-point systems 60 (*e.g.*, a multiple virtual lines (MVL) system, as is described in U.S. Patent No. 6,061,392 to Bremer *et al.*, which is incorporated herein by reference).

20   The symbol timing derivation systems 17, 66 described above can be implemented in software, hardware, or a combination thereof. In the preferred embodiment, the elements of the symbol timing derivation systems 17, 66 are implemented in software that is stored in a memory and that configures and drives a

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suitable digital signal processor (DSP), a variety of which are well known in the art,

situated in a modem. However, the foregoing software can be stored on any computer-

readable medium for transport or for use by or in connection with any suitable computer-

related system or method. In the context of this document, a computer-readable medium

5   is an electronic, magnetic, optical, or other physical device or means that can contain or

store a computer program for use by or in connection with a computer-related system or

method.

It should be emphasized that the above-described embodiments of the present

invention, particularly, any "preferred" embodiments, are merely possible examples of

10   implementations, merely set forth for a clear understanding of the principles of the

invention. Many variations and modifications may be made to the above-described

embodiments of the invention without departing substantially from the spirit and

principles of the invention. All such modifications and variations are intended to be

included herein within the scope of this disclosure and the present invention and

15   protected by the following claims.